HANGIL CHOI

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EDUCATION

Korea Advanced Institute of Science and Technology, Republic of Korea **Aug 2020 — Apr 2025 (Anticipated)**

- Ph.D in Electrical Engineering, Advised by Professor Seonghwan Cho
- Thesis: Subharmonic Injection-Locked Clock Multipliers with Low Reference Spur

Korea Advanced Institute of Science and Technology, Republic of Korea **Aug 2018 — Aug 2020**

- MS in Electrical Engineering, Advised by Professor Seonghwan Cho
- Thesis: A Fast FMCW Chirp Synthesizer Using Harmonic Compensation of VCO Nonlinearity

Yonsei University, Republic of Korea **Feb 2011 — Feb 2018**

- BS in Electrical & Electronic Engineering

PROJECT EXPERIENCE

Design of a High-Resolution 94GHz PLL with a 1GHz BW Using DFSS **Aug 2018 — Feb 2023**

- Electronics and Telecommunications Research Institute, Republic of Korea
- A 47GHz PLL and a frequency doubler were designed and measured for generating a 94GHz signal to be used in mm-wave military radar systems.

High Resolution Intelligent Radcomm System **Apr 2019 — Present**

- Institute of Information & communications Technology Planning & Evaluation, Republic of Korea
- A low-noise, low reference spur PLL was designed for radar and communication applications.

Low Jitter PLL with Versatile Frequency Modulation Capability **Sep 2020 — Present**

- Samsung Electronics, Republic of Korea
- An ultra low jitter injection locked clock multipliers were designed for recent communication.

PUBLICATIONS

- **H. Choi** and S. Cho, "A 7.5-GHz Subharmonic Injection-Locked Clock Multiplier Featuring a 120 × Multiplying Factor and 92.3-fs RMS Jitter Including Reference Spur," in IEEE Journal of Solid-State Circuits. (Early Access)
- **H. Choi** and S. Cho, "19.1 A 7.5GHz Subharmonic Injection-Locked Clock Multiplier with a 62.5MHz Reference, -259.7dB FoMJ, and -56.6dBc Reference Spur," 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 348-350.
- **H. Choi**, S. Lee and S. Cho, "Technique for Fast Triangular Chirp Modulation in FMCW PLL", IEICE Electronics Express, 2022, Volume 19, Issue 14, Pages 20220214.
- S. Lee, **H. Choi**, J. Lee, Kyu .Jung and S. Cho. "Evaluation and Analysis of High Temperature Characteristics of 94 GHz SiGe BiCMOS PLL" J. Korean Inst. Electromagn. Eng. Sci, 2023, Volume 34, no. 10, pp 743-746.

PATENTS

- **H. Choi**, S. Lee and S. Cho, “Phase-Locked Loop based Frequency Modulator That Can Perform Fast Modulation Independent of Bandwidth”, Korean Patent 10-2704944-0000 (2024)
- **H. Choi**, S. Lee and S. Cho, “Frequency modulation system based on phase-locked loop capable of performing fast modulation independent of bandwidth and method of the same”, US11632117B2 (2023)

INTEREST

- Analog Circuit Design, Phase-Locked Loop, Low Jitter Clock Multiplier, Wireless Communication